1. For the circuit shown below estimate the midband values for input resistance, output resistance, current gain, and voltage gain \( A_{V_{sm}} \).

\[ \beta_0 = 100 \]

2. Repeat problem 1 for the cases of Common Emitter with no bypass capacitor, Common Base, and Common Collector.

3. For the circuit shown below estimate the midband values for input resistance, output resistance, current gain, and voltage gain \( A_{V_{sm}} \).

\[ \beta_0 = 100 \]

4. Describe the trade-offs of using each of the 3 amplifier stages, i.e., common-emitter, common-base and common-collector for the BJT; and common-source, common-gate and common-drain for the FET.
5. For the circuit shown below estimate the midband values for input resistance, output resistance, current gain, and voltage gain ($A_{V_{sm}}$).

6. Repeat problem 5 for the cases of Common Source with no bypass capacitor, Common Gate, and Common Drain.

7. For the circuit shown below estimate the midband values for input resistance, output resistance, current gain, and voltage gain ($A_{V_{sm}}$).
8. For the cascaded 2-stage amplifier determine the midband values for input resistance, output resistance, current gain, and voltage gain ($A_{V_{sm}}$).

9. For the circuit shown below estimate the low frequency point at which $A_{V_{S}}$ becomes 0.707 of its maximum value. Also find the input impedance at 100 kHz.

10. For the circuit shown above estimate the high frequency point at which $A_{V_{S}}$ becomes 0.707 of its maximum value. Also find the input impedance at 100 kHz.
11. For the circuit shown below estimate the low frequency point at which $A_{VS}$ becomes 0.707 of its maximum value. Also find the input impedance at 100 kHz.

12. For the circuit shown above estimate the high frequency point at which $A_{VS}$ becomes 0.707 of its maximum value. Also find the input impedance at 100 kHz.

13. For the circuit shown below estimate the low frequency point at which $A_{VS}$ becomes 0.707 of its maximum value. Also find the input impedance at 100 kHz.

14. For the circuit shown above estimate the high frequency point at which $A_{VS}$ becomes 0.707 of its maximum value. Also find the input impedance at 100 kHz.

15. Describe how the Miller Transformation works and the conditions under which it is valid.
16. For the circuit shown below estimate the low frequency point at which $A_{vs}$ becomes 0.707 of its maximum value. Also find the input impedance at 100 kHz.

$$\begin{align*}
K &= 2.5 \text{ mA/V}^2 \\
V_p &= -2 \text{V} \\
V_s &= \text{VS} \\
R_D &= 360 \Omega \\
C_{gs} &= 3 \text{ pF} \\
C_{gd} &= 2 \text{pF} \\
\end{align*}$$

17. For the circuit shown above estimate the high frequency point at which $A_{vs}$ becomes 0.707 of its maximum value. Also find the output impedance at 100 kHz.

18a. For the BJT differential amplifier stage shown below, determine the CMRR.
b. If the 500 ohm emitter resistor is replaced with the active current source shown (lower left), once again determine the CMRR.
c. Comment on the improvement in CMRR obtained using the active current source.
19. Find the bias point of Q1 and determine the midband value of the voltage gain ($A_{Vs}$).

![Circuit Diagram]
Exam I practice problems  
EE3444, Summer 2008

Formula sheet

<table>
<thead>
<tr>
<th>Configuration/Parameter</th>
<th>$A_v$</th>
<th>$Z_{in}$</th>
<th>$Z_o$</th>
</tr>
</thead>
<tbody>
<tr>
<td>CE with feedback</td>
<td>$\frac{\beta R'<em>L}{r</em>{\pi} + (\beta + 1)R_E}$</td>
<td>$R_B \parallel (r_{\pi} + (\beta + 1)R_E)$</td>
<td>$R_C$</td>
</tr>
<tr>
<td>CE w/o feedback</td>
<td>$-g_m R'_L$</td>
<td>$R_B \parallel r_{\pi}$</td>
<td>$R_C$</td>
</tr>
<tr>
<td>CC</td>
<td>$\frac{(1 + \beta)R'<em>L}{r</em>{\pi} + (1 + \beta)R'_L}$</td>
<td>$R_B \parallel (r_{\pi} + (\beta + 1)R'_L)$</td>
<td>$R'E + r_{\pi} \parallel R_E$</td>
</tr>
<tr>
<td>CB</td>
<td>$g_m R'_L$</td>
<td>$R_E \parallel [r_{\pi}/(\beta + 1)]$</td>
<td>$R_C$</td>
</tr>
<tr>
<td>CS with feedback</td>
<td>$-\frac{g_m R'<em>L}{1 + g_m R</em>{\sigma}}$</td>
<td>$R_G$</td>
<td>$R_D$</td>
</tr>
<tr>
<td>CS w/o feedback</td>
<td>$-g_m R'_L$</td>
<td>$R_G$</td>
<td>$R_D$</td>
</tr>
<tr>
<td>CD</td>
<td>$\frac{g_m R'_L}{1 + g_m R'_L}$</td>
<td>$R_G$</td>
<td>$\left(\frac{1}{g_m}\right) \parallel R_{\sigma}$</td>
</tr>
<tr>
<td>CG</td>
<td>$g_m R'_L$</td>
<td>$\left(\frac{1}{g_m}\right) \parallel R_{\sigma}$</td>
<td>$R_D$</td>
</tr>
</tbody>
</table>

\[ g_m = \frac{I_{CQ}}{V_T} \quad g_m = \frac{\partial i_D}{\partial V_{GS}} \bigg|_{Qpt} \quad r_o = \frac{V_A}{I_{CQ}} \]

\[ I_D = k(V_{GS} - V_T)^2 = I_{DSS} \left(1 - \frac{V_{GS}}{V_{Tp}}\right)^2 \]

Effect of emitter bypass capacitor:

\[ f_1 = \frac{1}{2\pi R'_E C_E} \quad \text{and} \quad f_2 = \frac{1}{2\pi R'_E C_E} \quad \text{where} \quad R'_E = R_E \parallel \left(\frac{R_{\pi} + R_B \parallel R_S}{\beta + 1}\right) \]

(continued next page)

Formula sheet (continued)
Current source design equations

Simple current source $I_{ref} = \frac{V_{CC} + V_{EE} - V_f}{R_1}$

Widlar current source $I_o = \frac{V_T}{R_2} \ln \left( \frac{V_{CC} + V_{EE} - V_f}{R_1 I_o} \right)$

Wilson current source $I_o = \frac{V_{CC} + V_{EE} - 2 V_f}{R_1}$

Current source output impedances:

Simple current source $R_o = r_o$

Widlar current source $R_o = r_o (1 + g_m R_2)$

Wilson current source $R_o = \left( 1 + \frac{\beta}{2} \right) r_o$