Modern radios make heavy use of digital techniques. Sometimes the term 'software radio' is used where the digital techniques is (are) programmable as opposed to hardwired. Digital techniques have advantages in that some functions are difficult if not impossible to implement in an analog fashion. These include:
- FIR as opposed IIR filters
- equalization
- channel coding and decoding
- voice (image) coding and decoding
- pseudonoise (PN) coding and decoding
- timeslot synchronization

Digital techniques can be used to implement the functions in a straightforward manner. Digital techniques also offer greater stability in a component that performance depends largely on an accurate clock. To the
extent that a digital radio is programmable, i.e., implemented in software, it provides greater flexibility than conventional radios, e.g., wrt modulation type. We'll consider more about software radio shortly but first we'll examine some of the key digital components. It should be noted that there is a tendency to assume that digital components are ideal, and that digital
components, even ideal ones, don't have any substantial (negative) effects on the radio performance. It is important to first look at some characteristics of digital components.

Consider first basic aspects of a digital, in this case primarily software, radio. In this radio it is assumed that the DSP bank performs baseband filtering, demodulation, channel decoding, voice decoding, interleaving,
timeslot (or PN chip sequence) synchronization, symbol synchronization, and assistance in retrieval of control channel information.

Prescaler + divider ICs

For higher frequencies, below 1 GHz, BiCMOS and ECL have been used. Even if properly connected and used within stated frequency ranges, these
ICs influence phase noise via the addition of jitter. Jitter relates to the uncertainty of an event instant of an event relative to the expected (or average) instant of the event. For example, assuming a propagation delay of 1.5 ns for a particular IC, the event may actually occur at 1.5 ± .01 ns for 1000 measurements of the event.
The ±.01 ns represents one definition for jitter.

![Digital Device](Image)

Rising edge (≈ slope) defined as t=0. Measurements of rising edge propagation delay.

This jitter effect should be considered when designing PLL circuits since it will influence the phase noise. Jitter is a result of noise mechanisms within components of the digital device.
Analog-to-Digital Converters (ADC)

Even assuming ideal ADC with ideal S/H at the input there are effects introduced by a typical ADC that limit the performance of the receiver.

The dynamic range can be defined as:

$$20 \log \left( \frac{\text{max. voltage}}{\text{min. voltage}} \right)$$

$$= 20 \log \left( \frac{2^n}{1} \right)$$ where

n is the number of bits
used by the converter. So, for example, a 10-bit converter has a dynamic range of \( \log_2(1024) = 10 \) dB. This number by itself is not very meaningful since at very low counts the effective resolution, i.e.,

\[
\frac{\Delta V \text{ between counts}}{V}
\]

A better definition for dynamic range relates the maximum voltage to the minimum voltage that
maintains an acceptable resolution. Hence, the dynamic range (for good performance) is much lower than just stated. Resolution relates to the quantization noise, which is a result of not being able to exactly represent the input quantity. Consider the interpretation of $\frac{S}{N}$, where $N$ is the noise power resulting from the quantization. If the
maximum voltage representable is \( V_{\text{in}} \) and the waveform is sinusoidal, then \( S = \frac{V_{\text{in}}}{2} \). Now, if the quantization is to an accuracy of \( \pm V_e = \pm 0.5\Delta V \), and the probability of error is uniform within this interval then the noise power (the mean square error voltage) is

\[
N = \int_{-V_e}^{+V_e} \frac{g}{2V_e} \, dg = \frac{V_e^2}{3}
\]

If \( \frac{2V_{\text{in}}}{2\Delta V} = 2^n \), then
\[
\frac{S}{N} = \left( \frac{V_{in}^2}{2} \right) \left( \frac{3}{V_e^2} \right) = 1.5 \times (2^n)^2 \\
= 1.5 \times 2^{2n}
\]

\[
10 \log \left( \frac{S}{N} \right) = 10 \log \left( 1.5 \times 2^{2n} \right) \\
= \left( 1.76 + 6n \right) \text{ dB}
\]

For example, for a 10-bit ADC the quantization \( \frac{S}{N} \) is 61.76 dB. Notice, however, that this figure is valid (meaningful) only when the ADC is operating with peak...
values near the maximum count values of the ADC. Consider a 14-bit ADC such that the quantization noise must be $1 \geq 61.76$ dB. This implies that the dynamic range must be

$$20 \log\left(\frac{10384}{1024}\right) = 24$$ dB. For higher dynamic range either more bits must be used or the gain prior to the ADC
must be dynamically adjusted to hold the peak signal level so that at least 10 bits of the ADC are used.

The quantization aspect also implies that there is inherent nonlinearity that may be of importance for some applications. For single user devices, e.g., cell phones, the nonlinearity typically implies some distortion, i.e., generation of harmonics. However, if the
signal input to the ADC is a superposition of two or more signals, e.g., more typical of a base station environment, the quantization acts to cause some intermodulation distortion. The effects described until now are true of ideal and nonideal ADCs. Consider some additional effects that may occur due to nonideal characteristics.
The S/H is characterized by aperture uncertainty and aperture window. The processing being done usually assumes constant sampling interval, so this is a type of distortion. Also, some error is introduced if the ΔV between counts is not constant over the range of
the converter. This is generally a function of frequency and should be specified with the input signal at or near the Nyquist frequency with the ADC operating at its maximum sampling rate.

**Types of ADCs**

Flash converters - capable of very high speeds (hundreds of MHz) but complex. $2^n - 1$ comparators are required where $n$ is the number of bits.
Successive Approximation—

A DAC is used and its input is from a counter of \( n \) bits. When the DAC output equals the voltage of the signal input, conversion stops. Useful for 10s of MHz depending on number of bits used.

Slope converters—

These can have resolutions of 18 bits or so but are slow. They are not very
useful for communications. \( \Delta - \Sigma \) modulating converters

Instead of digitizing the voltage level input to the converter, this type of ADC digitizes only changes in the input signal level. It tends to operate at sampling rates that are much higher than standard ADCs, i.e., sampling at
rates much greater than the Nyquist rate. Typically Δ-Σ converters have a one-bit resolution such that if digitization of a voltage input is needed, several cycles are required. In some applications, though, the Δ (difference) value is all that is required. Consider the block diagram:
As an example of performance consider the response to a ramp input.

Figure 1.5 The response of a multilevel ΔΣ quantizer to a ramp input. A two-level response is obtained by curtailing input amplitude to a range of values that lies between two adjacent quantization levels.

(From Delta-Sigma Data Converters, IEEE Press, 1996)
One advantage of Δ-Σ modulators is the ability to shape the noise spectrum. For frequency components lying \( \ll \frac{fs}{2} \) the noise (quantization noise) is greatly reduced. The
noise at higher frequencies can be removed via the use of digital filtering (more later).

Advantages
- circuit is simple
- inherently monotonic
- inherently linear
- no S/H required
- minimal antialiasing filter
- background noise level is independent of input signal level.
- Quantization noise can be effectively filtered.

Disadvantages:
- Primary disadvantage is with operating speed.

Digital-to-analog converters (DACs):

Once again, this is inherently nonlinear. Harmonics of the input signal appear, but generally can be filtered. Aliasing effects...
also occur. Aliasing effects can occur as a result of multiplication of the rectangular sampling intervals with the desired signal. Other spurious responses can appear if the device is nonmonotonic. At higher sampling rates spurious may appear as a result of skew rate limiting.
of op amps, switches
(on the R-2R ladder) not
closing or open at the
same instant. As a
result DACs are
commonly specified in
terms of spurious free
dynamic range (SFDR),
third harmonic distortion
(THD) and S/N or SINAD.

Processing elements
DSP devices are commonly used largely due to their programming flexibility. But other options exist:

- PLD for higher speed processing aspects (FFT) or a particular voice coding or decoding algorithm, etc.

A variety of DSP
devices exist. Some are fixed point, while some applications require floating point. Some DSP devices have been tailored for a particular type of communication and may include dedicated functions and programmable DSP on the same IC.