Problem 4.51

Dc circuit:

\[ V_{BEQ} = 0.7 \, \text{V} \]
\[ \beta = 100 \]

\[ V_B = V_{CC} \frac{R_2}{(R_1 + R_2)} = 7.5 \, \text{V} \quad R_B = R_1 \parallel R_2 = 5 \, \text{k}\Omega \]

\[ I_{BO} = \frac{V_B - V_{BEQ}}{R_B + (\beta + 1)R_E} = 64.1 \, \mu\text{A} \quad I_{CQ} = \beta I_B = 6.41 \, \text{mA} \]

\[ r_n = \frac{\beta V_T}{I_{CQ}} = 405 \, \Omega \quad R'_L = R_L \parallel R_E = 333 \, \Omega \]

\[ A_v = \frac{R'_L(\beta + 1)}{r_n + R'_L(\beta + 1)} = 0.988 \quad A_{vo} = \frac{R_E(\beta + 1)}{r_n + R_E(\beta + 1)} = 0.996 \]

\[ Z_{in} = R_B \parallel [r_n + R'_L(\beta + 1)] = 4.36 \, \text{k}\Omega \]

\[ A_i = A_v Z_{in}/R_L = 8.61 \quad G = A_v A_i = 8.51 \]

\[ R'_s = R_B \parallel R_s = 833 \, \Omega \]

\[ Z_o = R_E \parallel [(R'_s + r_n)/(\beta + 1)] = 12.1 \, \Omega \]
Problem 5.47

We have

\[ K = \left( \frac{w}{L} \right) \frac{K^2}{2} = 400 \ \mu A/V^2 \]

Assuming operation in saturation, we have

\[ I_{DQ} = K (V_{GSQ} - V_{to})^2 \]

Solving for \( V_{GSQ} \) and evaluating we have

\[ V_{GSQ} = V_{to} + \frac{I_{DQ}}{K} = 3.236 \ V \]

\[ V_G = V_{DD} \frac{R_2}{R_1 + R_2} = 10 \ V \]

\[ V_G = V_{GSQ} + R_S I_{DQ} \]

Solving for \( R_S \) and substituting values we have

\[ R_S = \frac{(V_G - V_{GSQ})}{I_{DQ}} = 3.382 \ k\Omega \]

We have \( g_m = \sqrt{K I_{DQ}} = 0.8944 \ \text{mS} \)

\[ R_L' = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + \frac{1}{R_L}} = 1.257 \ k\Omega \]

\[ A_v = \frac{V_o}{V_{in}} = \frac{g_m R_L'}{1 + g_m R_L'} = 0.5293 \]

\[ R_{in} = \frac{V_{in}}{I_{in}} = \frac{R_G}{R_1 || R_2} = 666.7 \ k\Omega \]

\[ R_o = \frac{1}{g_m + \frac{1}{R_S} + \frac{1}{r_d}} = 840.0 \ \Omega \]
Problem 7.10

The circuit diagram is shown below. We returned R to ground rather than to $+V_{CC}$, so the value of R would be smaller and require less chip area. The transistors both have relative areas of unity. Initially we selected $R = (V_{EE} - 0.6)/I_{ref} = (14.4 \text{ V})/(0.5 \text{ mA}) = 28.8 \text{ k}\Omega$. Then we simulated the circuit and adjusted R to attain $I_O \approx 0.5 \text{ mA}$ for $V_O = 0$.

![Circuit Diagram]

The simulation is stored in the file named P7_10. For $V_O$ ranging from -5 to +5 V the current ranges from 0.462 to 0.540 mA. The output resistance is 128.5 k\Omega.
Problem 7.12

The circuit diagram is shown on the next page. We returned R to ground rather than to \(+V_{CC}\) so the value of R would be smaller and require less chip area. The transistors all have relative areas of unity. Initially we selected \(R = (V_{EE} - 1.2)/I_{ref} = (13.8\ \text{V})/(0.5\ \text{mA}) = 27.6\ \text{k}\Omega\). Then we simulated the circuit and adjusted R to attain \(I_O = 0.5\ \text{mA}\) for \(V_O = 0\).

The simulation is stored in the file named P7_12. For \(V_O\) ranging from \(-5\) to \(+5\ \text{V}\) the current ranges from 0.49807 to 0.49948 mA. The output resistance is 7.12 M\Omega.
Problem 7.24

(a) \( I_1 = (V_{CC} - 2V_{BE})/R_1 \)

\[ I_{C3} = I_{C1} = I_1 - I_{B2} \]

\[ = I_1 - I_{E2}/(\beta + 1) \]

\[ = I_1 - (I_{B1} + I_{B3})/(\beta + 1) \]

\[ = I_1 - 2I_{C3}/[\beta(\beta + 1)] \]

\[ I_{C3} = \frac{(V_{CC} - 2V_{BE})\beta(\beta + 1)}{R_1(\beta^2 + \beta + 2)} \]

(b) Evaluating we have

<table>
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<tr>
<th>( \beta )</th>
<th>( I_{C3} ) (mA)</th>
<th>Percentage increase = 0.0033%</th>
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<tr>
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<td>0.453244</td>
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<tr>
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(c) For the current mirror of Figure 7.1 we have \( I_{ref} = (V_{CC} - V_{BE})/R \) and \( I_{C2} = I_{ref}/(1 + 2/\beta) \). Evaluating we have

<table>
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<th>( \beta )</th>
<th>( I_{C2} ) (mA)</th>
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<td>110</td>
<td>0.468154</td>
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</table>

(d) The compliance range is \( V_o > 0.2 \) V.
Problem 7.46

Many correct answers exist. One is shown below.

For simplicity we have replaced the current source with $R_E$ and eliminated the resistor in the collector of $Q_1$. When $Q_1$ is off, the voltage at the emitter of $Q_2$ is approximately $-0.6$ V. For zero output voltage we need $I_{E2} = I_{C2} = 15/R_C = 1.5$ mA. Thus we need $R_E = (15 - 0.6)/I_{E2} = 9.6$ kΩ. When $Q_2$ is off, $R_C$ and $R_L$ act as a voltage divider producing $v_o = 5$ V. The simulation is stored in the file named P7_46.
Problem 7.60

Many correct answers can be found. Here is one example:

![Circuit Diagram]

The simulation is stored in the file named P7.60. (Actually, two versions of the circuit are simulated: one for the differential gain and the other for the common-mode gain.) At 60 Hz, the simulation yields $A_{\text{vd}} = 10$ dB and $A_{\text{cm}} = -67$ dB for a CMRR of 77 dB. Resistor $R_{D1}$ is included so the bias points are identical for $J_1$ and $J_2$, which makes the circuit more balanced and reduces $A_{\text{vcm}}$. 