Output Stages

Section 5

Amplifier Classes

Class A Amplifier
If the signal current is

\[ i_0 = \hat{I}_C \sin \omega t \]

and the bias current is \( I_C \), then the total current is

\[ I = I_C + \hat{I}_C \sin \omega t. \]

For the class A amplifier, \( \hat{I}_C < I_C \), so that the entire waveform of the AC signal is amplified without distortion. The conduction angle is 360°.

Class B amplifier
In this case, the bias current, \( I_C = 0 \). Since the transistor is cutoff when the total voltage is less than 0, only the positive half of the wave is amplified. The conduction angle is then 180°. Ordinarily in this case, another transistor amplifies the negative half cycle and the two halves are put together again.

Class AB amplifier
For the Class AB amplifier, the DC bias current is much smaller than the signal amplitude, \( \hat{I}_C \), but still greater than 0. In this case,

\[ 180^\circ < \text{conduction angle} < 360^\circ. \]

Class C amplifier
In the class C amplifier, the DC bias current is negative, i.e. \( -I_C \). Thus the conduction angle < 180°.

Characteristics of Output Stages
1. Large current and voltage swing
2. Low output impedance
3. Low standby power.

The second characteristic normally demands use of an emitter follower connection. One fairly simple circuit consists of a driver or input transistor Q1 that is biased by a current source in its collector, and an output transistor Q2 whose base is connected to the
collector of Q1. Q2 is also biased by a current source, \( I_{EE} \) in its emitter. The load, \( R_L \) is also taken off the emitter. In this case, the approximate output resistance is

\[
R_{out} \approx \frac{1}{g_m} + \frac{R_A}{\beta}
\]

where \( R_A \) is the effective resistance in the base of the output transistor (Q2). The advantages of this circuit are
1. It is a simple, stable circuit.
2. It has low distortion.
3. It has low output impedance.

The disadvantages of this circuit are
1. It has high standby power.
2. It has unsymmetrical current drive.

The high standby power is a result of the current source \( I_{EE} \) in the emitter which is always on even when there is no input signal. The maximum current through the load is

\[
I_{max}^+ = \frac{V_{CC} - V_{EC4-sat} - V_{BE2}}{R_L}
\]

The emitter-collector voltage of Q4 is a result of current mirror supplying bias current \( I_B \) to the collector of Q1. The transistor Q4 goes into saturation before the output transistor Q2 does. In the negative direction, the maximum output current is

\[
I_{max}^- = -I_{EE}
\]

Consequently, the current swing is not necessarily symmetrical.

A variation on this theme is the totem pole circuit that has in addition to the previous circuit two diodes, one in the collector of Q1 and the other in the emitter of Q2. The diode in the emitter of Q2 replaces the current source \( I_{EE} \) used in the previous circuit. For positive output current, the current is drawn from positive bias supply, \( V_{CC} \) as before. For negative output current, the driver transistor, Q1, draws the current from the load and directs it down to the negative bias supply, \( V_{EE} \).

An improvement in this circuit makes use of a composite transistor composed of two npn transistors Q3 and Q1. While the composite transistor was described earlier, it may be worth while reviewing it. The base and collector of Q3 is connected directly to the base of Q1, and emitters of Q1 and Q3 are connected together. The transistor Q1 is considered the main output transistor. The collector current of the composite transistor is \( I'_C = I_{C1} \). For Q3,

\[
I_{B3} = \frac{I_{C3}}{\beta_3}
\]

The base current of the composite transistor is

\[
I'_B = I_{B1} + I_{C3} + I_{B3} = \left( \frac{1}{\beta_3} + 1 \right) I_{C3} + \frac{I_{C1}}{\beta_1}
\]
Since Q1 draws the major amount of current, its cross sectional area $A_1$ is larger than that of Q3, $A_3$. This will affect the base-emitter voltages of these two transistors.

$$V_{BE1} = V_t \ln \frac{I_{C1}}{I_{S1}} = V_{BE3} = V_t \ln \frac{I_{C3}}{I_{S3}}$$

This implies

$$I_{C3} = \frac{A_3}{A_1} I_{C1}$$

This is substituted back into the equation for the composite base current.

$$I'_B = \left( \frac{1}{\beta_3} \right) \frac{A_3}{A_1} I'_C + \frac{I'_C}{\beta_1}$$

This is then solved for the composite collector current, $I'_C$.

$$I'_C = \frac{I'_B}{\frac{A_3}{A_1} \left( 1 + \frac{1}{\beta_3} \right) + \frac{1}{\beta_1}}$$

$$= \frac{A_3}{1 + \frac{1}{\beta_3} + \frac{A_1}{A_3 \beta_1}} I'_B$$

If it is assumed that $\beta_1 = \beta_3 = \beta$, which is not that good of an assumption because of the large difference in their current carrying capacity, then

$$I'_C \approx \frac{A_1}{A_3} I'_B \left[ 1 - \frac{1}{\beta} \left( 1 + \frac{A_1}{A_3} \right) \right]$$

$$\approx I'_B \frac{A_1}{A_3}$$

It is this equation that is used in the composite transistor version of the class B amplifier.

**Complementary Class B Stage (Push Pull)** If instead of using two npn transistors, one of them can be replaced by a pnp transistor. Although the integrated circuit pnp transistor cannot be made to perform at the same level as an npn, the symmetry of the complementary circuit has much to offer.

In this circuit, the npn transistor Q1 has its collector connected to the positive power supply, $V_{EE}$ and its emitter connected to the load, $R_L$. The collector of the pnp output transistor, Q2, has its collector connected to the negative supply voltage $V_{EE}$ and its emitter also connected to the load, $R_L$. The bases of Q1 and Q2 are connected together and are driven by the collector of the input transistor Q3. As before, the input transistor, Q3, has a bias current source, $I_B$ feeding its collector (and also provides base current for Q1). The input voltage, $V_{in}$ to the input transistor Q3 is what drives the output stage. It is tempting when doing hand or SPICE calculations to start with $V_{in}$. However, because a small change in base voltage of Q3 makes a large change in the collector voltage of Q3, it is easier to start the analysis at the bases of Q1, Q2. This base voltage can be called $V_b$. 

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When \( V_b = 0 \), both the output transistors Q1 and Q2 would be turned off because the voltage is less than the 0.6 Volts necessary to turn the transistors on. If \( V_b > 0.6 \), then Q1 (npn) is on and Q2 (pnp) is off. Current is then drawn from \( V_{CC} \) through Q1 to produce the positive half wave of the signal in the load, \( R_L \). If \( V_b < 0.6 \), then Q1 (npn) is off and Q2 (pnp) is on. \( V_b \) is made negative by turning Q3 on thus bringing the collector voltage of Q3 closer to \(-V_{EE}\). An extreme positive or negative voltage puts the turned on transistor into saturation. The maximum positive output voltage is

\[
V_{out}^+ = V_{CC} - V_{CE1(sat)}
\]

and the maximum negative output voltage is

\[
V_{out}^- = -V_{EE} + V_{EC2(sat)}.\]

In this case, the voltage gains are

\[
A_v^+ \approx -g_{m3} \beta_1 R_L \\
A_v^- \approx -g_{m3} \beta_2 R_L.
\]

The gain in this circuit is more symmetrical than the previous totem pole all npn circuits described earlier, particularly when \( V_{CC} = -V_{EE} \).

When the current source is replaced by a resistor, \( R_1 \), the maximum output voltage across the load is

\[
V_{out}^+ = \frac{V_{CC} - V_{BE1}}{1 + \frac{R_1}{\beta_1 R_L}} \\
\approx 0.98(V_{CC} - V_{BE1}).
\]

**Small Signal Analysis**

Returning to the generic complementary class B output stage, where \( R_1 \) is returned back to a DC current source, \( I_B \), Q1 is the npn output transistor, Q2 is the pnp output transistor and Q3 is the driver transistor (also npn), a small signal analysis is to be performed. The goal now is to find the voltage gain, \( R_{in} \) and \( R_{out} \). Since neither Q1 nor Q2 are on simultaneously, only one need be considered at a time. Assuming that Q1 is on, Q2 is an open circuit and need not be considered as part of the AC analysis. Since the voltage gain of the emitter follower is

\[
A_v = \frac{1}{1 + \frac{R_{bb} + r_{b1} + r_{e1}}{R_L || r_{o1} (r_{e1} + 1)}} \\
\approx 1
\]

the voltage gain of the entire two transistor section is the product of the common emitter gain and the emitter follower gain (=1). The output voltage across the load resistor, \( R_L \) is

\[
V_{out} = -g_{m3} R_L (\text{eff}) V_{in}.
\]
The effective load resistance $R_{L(\text{eff})}$ seen by the first transistor, Q3, is the same as the input resistance of the emitter follower circuit Q1.

$$R_{L(\text{eff})} = R_{\text{in}-\text{ac}} = r_{\pi 1} + r_{b1} + (\beta_1 + 1)(r_{e1}||R_L)$$

$$\approx \beta_1 R_L$$

The voltage gain is then found by substitution.

$$A_v^+ = -g_{m3}[r_{\pi 1} + r_{b1} + (\beta_1 + 1)(r_{e1}||R_L)]$$

$$\approx -g_{m3}\beta_1 R_L$$

**Elimination of the Dead Band** The 1.2 to 1.4 volt range in the base voltages of Q1 and Q2 can be substantially compensated by addition of two diodes in series between the base of Q1 and that of Q2. These diodes are named respectively D3 and D4. For purposes of calculation, let $V_i$ stand for the voltage at the collector of the driver transistor Q3 which is the same as the base voltage for the pnp output transistor Q2. To get to the base of Q1 from $V_i$ now requires going through the two series connected diodes “backwards” from cathode to anode. If $V_i > 0$ but not so high as to turn off the diodes D3 and D4, then Q1 is on (as in the earlier circuit described above without the diodes). The voltage across the load is

$$V^+_{\text{out}} = V_i + V_{D4} + V_{D3} - V_{BE1}.$$}

When $V_i < 0$, the input voltage to the driver Q3 becomes a positive voltage. The npn output transistor Q1 is turned off and the excess bias current source drawing current positive power supply puts all into the diodes D3 and D4 and then through the now turned on Q3. The output voltage is not affected directly by the diodes now, so

$$V^-_{\text{out}} = V_{EB2} + V_i$$

where the value of $V_i$ is actually a negative number. In the middle when $V_i = 0$,

$$V^+_{\text{out}} = V_{D4} + V_{D3} - V_{BE1} \approx V_{BE}$$

$$V^-_{\text{out}} = V_{BE2} = V_{BE}.$$
Q1 need be considered. This transistor carries only the positive half of a sine wave. The other half of the time it is turned off. The average current drawn from the supply over a full cycle is given as follows.

\[
I_{\text{supply}} = \frac{1}{T} \int_0^{T/2} \dot{I}_C \sin \omega t \, dt = -\frac{\dot{I}_C}{\omega T} \cos \omega t \bigg|_0^{T/2} = -\frac{\dot{I}_C}{\frac{2\pi}{T}} \left[ \cos \left( \frac{2\pi T}{2} \right) - 1 \right] \bigg|_0^{T/2} = -\frac{\dot{I}_C}{2\pi} [-1 - 1] = \frac{\dot{I}_C}{\pi} = \frac{1}{\pi} \frac{V_{\text{out}}}{R_L}
\]

The power drawn from both of the power supplies by both of the output transistors is

\[
P_{\text{supply}} = 2V_{\text{CC}} I_{\text{supply}} = \frac{2V_{\text{CC}}}{\pi} \frac{V_{\text{out}}}{R_L} \cdot V_{\text{out}}
\]

Thus, the output power is proportional to \( V_{\text{out}} \). This is the average power drawn from the power supply. The power delivered to the load is

\[
P_L = \frac{|V_{\text{out}}|^2}{2R_L}
\]

The efficiency is the ratio of these latter two values.

\[
\eta = \frac{P_L}{P_{\text{supply}}} = \frac{|V_{\text{out}}|^2 \frac{\pi}{2} \frac{R_L}{2V_{\text{CC}}V_{\text{out}}}}{2R_L} = \frac{\pi V_{\text{out}}}{4V_{\text{CC}}}
\]

The maximum output power occurs when \( V_{\text{out-max}} = V_{\text{CC}} - V_{\text{CE(sat)}} \).

\[
P_{L(\text{max})} = \frac{1}{2} \left( V_{\text{CC}} - V_{\text{CE(sat)}} \right)^2 \frac{R_L}{2} \\
\eta_{\text{max}} = \frac{\pi}{4} \frac{V_{\text{CC}} - V_{\text{CE(sat)}}}{V_{\text{CC}}} \approx 78.5\%
\]

This efficiency for the class B amplifier should be compared with the maximum efficiency of a class A amplifier where \( \eta_{\text{max}} = 25\% \).

The 741 Op. Amp Output Stage
Since the diodes used in compensation for the dead band carry much less power than the output transistors, the diodes are typically much smaller in cross sectional area. Better match between the output transistors and the diodes could be accomplished by simply allowing the diodes to carry more current. However, in so doing, a compromise is being made in the crucial property of efficiency. A better solution is to replace the diodes with emitter follower circuit consisting of Q18, Q19, Q23 (pnp), the driver transistor Q17, and $R_{10}$ in the 741 operational amplifier. The transistor Q13A is the current source from a current mirror and provides 0.22 mA of current. When the base voltage, $V_{in}$ to Q17 is positive, the base voltage of Q23, $V_{B23}$ goes down and Q23 (pnp) turns on. Current flows from the load through the pnp output transistor, through Q23 and finally through Q17 to the negative power supply. As a result, 

$$V_{out}^- = -V_{CC} + V_{EB20} + V_{EB23} + V_{CE17(sat)}.$$  

The minimum (maximum negative) voltage is \(\approx 1.4\) volts less than \(| - V_{CC}|\). When $V_{in}$ is negative, Q17 turns off raising its collector voltage high. This in turns off the pnp Q23 forcing the current from the mirror Q13A to feed the base of Q14 (the output npn transistor). Eventually, Q13A being smaller than Q14, goes into saturation. As a result, the maximum positive voltage at the output is given by 

$$V_{out}^+ = V_{CC} - V_{BE14} - V_{CE13A(sat)}$$

which is about 0.8 volts below $V_{CC}$.

Now if for power transistor Q14, $\beta_{14} = 100$, then the output current in the load is 

$$I_{out} = \beta_{14} I_{C13A} = 100 \cdot 0.22 \text{ mA} = 22 \text{ mA}.$$  

In the original diode circuit, the diodes forward voltage drop was supposed to compensate for the $V_{BE}$ drop of the transistors. But, because the diode areas are smaller than the output devices (Q14 and Q20 in the 741 operation amplifier), 

$$V_{BE14} = V_{BE20} < V_{D3} = V_{D4}.$$  

What is needed in effect a smaller $V_D$ for the equivalent diode circuit. The substitution is Q18, Q19, and $R_{10}$. This arrangement still provides two base-emitter voltage drops across the bases of the output power transistors. But the emitter current of Q19 is small since all it does is feed the base current for Q18 plus a small bleeder current through $R_{10}$. The emitter current of Q19 goes into $R_{10}$ and into the base of Q18, 

$$I_{E19} = I_{R10} + I_{B18}$$  

The value for $R_{10}$ is a rather large 40 kΩ. Hence the total current drawn by Q18 and Q19 is less than what would be needed by two diodes. Now, 

$$V_{BE18} + V_{BE19} < V_{D3} + V_{D4}$$
The challenge now is to determine what could make
\[ V_{BE_{18}} + V_{BE_{19}} = V_{BE_{14}} + V_{EB_{20}}. \]
Making use of the Shockley diode equation, the above expression becomes
\[ V_t \left( \ln \frac{I_{C_{19}}}{I_{S_{19}}} + \ln \frac{I_{C_{18}}}{I_{S_{18}}} \right) = V_t \left( \ln \frac{I_{C_{14}}}{I_{S_{14}}} + \ln \frac{I_{C_{20}}}{I_{S_{20}}} \right). \]
Since \( I_{C_{14}} = I_{C_{20}} \) at least under open circuit load conditions,
\[ \frac{I_{C_{19}} I_{C_{18}}}{I_{S_{19}} I_{S_{18}}} = \frac{I_{C_{14}}^2}{I_{S_{14}} I_{S_{20}}}. \]
Solving this for the output current gives
\[ I_{C_{14}} = -I_{C_{20}} = \sqrt{I_{C_{19}} I_{C_{18}}} \sqrt{\frac{I_{S_{14}} I_{S_{20}}}{I_{S_{18}} I_{S_{19}}}}. \]
If \( \beta_1 \) is large, most of the Q19 emitter current is the same as the collector current. Relatively little of this feeds the base current of Q18. The current going through the bleeder resistor \( R_{10} \) is
\[ I_{C_{19}} = \frac{V_{BE_{18}}}{R_{10}} \approx \frac{0.6}{40k\Omega} = 15\mu A. \]
Neglecting base currents for Q14 and Q20,
\[ I_{C_{18}} = I_{C_{13}A} - I_{C_{19}} = 220 - 15\mu A = 205\mu A. \]
Knowing these values and the saturation currents, the value for output current \( I_{C_{14}} \) is found. Typical value for the 741 operational amplifier gives \( I_{C_{14}} = 0.16mA \)

**Current Limiting**

The main goal of the current limiting circuit is to prevent burn out of the output transistors Q14 and Q20 in the operational amplifier when the load draws too much current such when the load is short circuited to ground. The idea is to add a transistor that would shunt the base current say for Q14 in the output stage around directly to the load. The high power transistor is prevented from carrying too much current. The “overload” is a the much smaller base current is simply dumped into the load. To do this another transistor, Q15, is added so that the collector of Q15 is connected to base of Q14, the emitter of Q15 is connected to \( R_L \) and the base of Q15 is connected to the emitter of Q14. In addition a small resistor, \( R_6 \) is added between the emitter of Q14 and \( R_L \). This resistor is typically only 27\( \Omega \) so it should not affect the circuit since it is much smaller than typical load resistances \( R_L \). The added transistor Q15 ordinarily is off. Only when the current drawn through added Q14 emitter resistor \( R_6 \) gets large enough to cause the \( V_{BE_{15}} \) to rise above 0.6 volts does Q15 turn on and start shunting current away from the base of the power transistor. Resistor \( R_6 \) is used to sense the output current. The maximum load current then is easily found.

\[ I_{L(max)} = \frac{V_{BE(on)}}{R_6} \]

When the load current reaches this value, Q15 starts to conduct the base current away from Q14 and on into the load. This technique must be modified somewhat for the pnp case.