6.1 The Operational Amplifier as a Circuit Element

The ideal operational amplifier has $\infty$ input impedance, 0 output impedance, and $\infty$ voltage gain. The usual procedure in analyzing a circuit with one or more operational amplifiers is to always start at the input side of the operational amplifier and write node equations there. Writing node equations at the output side is not fruitful since the output impedance is so low. If the operational amplifier is connected as an inverting amplifier, with $Z_1$ at the input side connecting directly to the (-) terminal of the operational amplifier and $Z_f$ connected between the inverting input terminal and the output. If the operational amplifier has an input impedance $Z_{in} \neq \infty$, an open loop voltage gain $-A \neq \infty$ and an output impedance $= 0$, then the overall amplifier voltage gains is given as follows.

\[
\begin{align*}
V_1 &= Z_1 I_1 + V_{in} \\
V_{out} - V_{in} &= I_f Z_f \\
V_{in} &= Z_{in} (I_1 + I_f) \\
V_{in} &= -\frac{V_{out}}{A}
\end{align*}
\]

\[
\begin{align*}
V_1 &= I_1 Z_1 - \frac{V_{out}}{A} \Rightarrow I_1 = \frac{V_1 + V_{out}/A}{Z_f} \\
V_{out} \left(1 + \frac{1}{A}\right) &= I_f Z_f \Rightarrow I_f = \frac{V_{out} + 1/A}{Z_f} \\
V_{in} &= Z_{in} \left[\frac{V_1 + V_{out}/A}{Z_1} + \frac{V_{out}(1 + 1/A)}{Z_f}\right]
\end{align*}
\]

In the last equation, substitute for the value for $V_{in}$ in the first set of equations and solve for $V_{out}$.

\[
\begin{align*}
-\frac{V_{out}}{A} - Z_{in} V_{out} &= \frac{Z_{in}}{Z_f} V_{out} \left(1 + \frac{1}{A}\right) = \frac{Z_{in}}{Z_1} V_1 \\
A_v = \frac{V_{out}}{V_1} &= -\frac{Z_f}{Z_1} \frac{1}{1 + \frac{1}{A} \left(1 + \frac{Z_f}{Z_1} + \frac{Z_f}{Z_{in}}\right)}
\end{align*}
\]
If $Z_f = \infty$, the voltage gain is

$$A_v = -\frac{AZ_{in}}{Z_{in} + Z_1}$$

where $A_v$ is typically some reasonable value like 10 dB, and the open loop gain, $A$ can be very large. When $A \to \infty$,

$$A_v = -\frac{Z_f}{Z_1}.$$ 

The input voltage across the two input terminals is zero in the ideal case. The reason for this strange behavior is because of the infinite gain.

$$V_{in} = -\frac{V_{out}}{A} \to 0$$

In this case, the circuit will move its output to whatever voltage is necessary to drive $V_{in}$ to 0.

Typically, the input resistance is 100 kΩ, to 1 MΩ, the output resistance is 40 to 100 Ω, the unity gain bandwidth is 1 to 20 MHz, and the low frequency gain $A$ is 60 dB. The offset current is typically $I_{os} \approx 0.5 \mu A$.

Depending on the input and feedback impedances, the following circuits can be designed.

- Inverting amplifier
- Summing amplifier
- Noninverting amplifier
- Log amplifier
- Exponential amplifier
- Integrator
- Differentiator

**Deviations from Ideality**

1. Nonzero input bias current

   The input stage current is $I_{Bias} = (I_{B1} + I_{B2})/2$. For BJT operational amplifiers this is approximately 10 to 100 nA. For MOS operational amplifiers this is approximately 0.001 pA. Clearly, the MOS circuits are superior regarding this parameter. This current can cause undesired voltage drops in external resistors.

2. Input offset current, $I_{os}$

   The value for the offset current is $I_{os} = I_{B1} - I_{B2}$.

3. Input offset voltage, $V_{os}$

   This is the voltage needed to drive the output to 0 V. For a BJT amplifier, $V_{os} \approx 0.1$ to 2 mV. For a MOS amplifier this is 1 to 20 mV. The offset voltage plus the temperature drift limits the dc accuracy.

4. Common Mode Input Range (CMIR)

   This is the range common mode input voltages for which an operational amplifier behaves within specifications.

5. Common Mode Rejection Ratio (CMRR)
The operational amplifier has a differential input and a single-ended output so that the output is $\propto V_{ID}$ and $V_{IC}$. The output voltage is proportional to both these voltages.

$$V_o = A_{dm}V_{ID} + A_{cm}V_{IC}$$

so that

$$CMRR = \left| \frac{A_{dm}}{A_{cm}} \right|$$

This is the same as the change in input $V_{os}$ that results from change from a common mode input voltage. See text for derivation.

$$CMRR = \left| \frac{A_{dm}}{A_{cm}} \right| = \left| \frac{\Delta V_{os}}{\Delta V_{IC}} \right|$$

6. Power Supply Rejection Ratio (PSRR)

PSRR is the variation in $V_o$ that occurs with changes in supply voltage.

6.2 Block Diagram of an Operational Amplifier

Single Stage Operational Amplifier

This circuit consists of a single input differential amplifier stage that provides the gain and whose output is single ended. The output feeds into a buffer amplifier whose gain is 1. Between the two is a shunt capacitor to ground that is used to insure stability for all values of feedback. The gain of this circuit is $A_v = g_m (r_{o1} || R_{i2})$ where $r_{o1}$ is the output resistance of the first stage and $R_{i2}$ is the input resistance of the buffer amplifier.

Class Two Stage Operational Amplifier

The first stage is a differential amplifier that provides gain and converts the differential input to a single ended output. The second stage is a common emitter type stage that provides significantly more gain. This again feeds into the class B buffer stage. A capacitance is used between the input and output of the middle amplifier to help stabilize the circuit. It provides a single pole of frequency roll off and can be made to prevent instability for any values of external passive feedback. Some operational amplifiers are not so robust so as to allow a designer to do his own stabilization. The most common operational amplifier, the $\mu$A741 is of this type. The two differential input transistors in the first stage deliver their outputs into the emitters of pnp transistors. The combination acts like a composite transistor. Since the output is at a lower bias level than the input, there is also level shifting taking place. This is done to avoid using expensive DC blocking capacitors between stages.

The second stage is an inverter circuit with an active load. Its function is to provide more gain. The output of this stage is fed into the driver transistor for the class B amplifier.

Three Stage Operational Amplifier

The input consists again of a differential amplifier. There follows two inverter circuits with some feedback and feed forward elements for stability purposes. This feed again into a class B output amplifier. This particular circuit will not be discussed here, but does alert us that there a variety of types of operational amplifiers.
6.3 DC Analysis of the $\mu$A741 Operational Amplifier

The $\mu$A741 operational amplifier has a fairly standardized numbering for transistors and resistors. The circuit diagram is shown in the figure.

The first stage of the $\mu$A741 provides the following functions.

1. Provide differential input that is insensitive to common mode voltages, that has high input impedance, and has some voltage gain.
2. Level shifting to be accomplished by using lateral pnp transistors in the signal path. The pnp transistors have their collectors near the negative supply voltage.
3. Provide a conversion from the differential input to a single ended output. This is done by taking the output from the collector of one of the differential transistors.

The second stage is an emitter follower which provides a high input impedance. This reduces loading to the first stage. The output buffer provides no voltage gain, but does provide high power handling.

Bias Currents

The wrong approach is to assume that the two input terminals are grounded and try to predict the output voltage. Any small variation in $\beta$ somewhere will make a large change in the output voltage $V_{out}$ so that the output transistors might not be in the active region. The solution is to assume that the circuit has a specified $V_{out}$ which is usually 0. For hand calculations, it is useful to assume the transistor Early voltage resistances, $r_o$ are all infinite. This will not greatly affect the DC current values nor the AC calculations later on. The basic approach is to find all the DC collector currents for the transistors. This will allow calculation of the $g_m$’s for the transistors. The next step is to apply the hybrid equivalent circuit model for the transistors and do the AC calculation for gain.

The numbering of transistors for the $\mu$A741 is fairly standardized so a circuit drawing
from any source will be the same. The key to unlocking this circuit is found in recognizing that the voltage across \( R_5 \) is merely the difference between the high and low supply voltages minus the \( V_{BE} \) voltage drops of Q11 and Q12. If the supply voltages are +15 and -15 volts, and the transistors Q11 and Q12 are in their active region the current \( I_B \) flowing through \( R_5 \) is

\[
I_B = \frac{V_{CC} - (-V_{EE}) - 2V_{BE(on)}}{R_5} = \frac{30 - 1.4}{39 \, \text{k}\Omega} = 0.73 \, \text{mA}.
\]

The transistors Q11 and Q10 form a Widlar current source which was described previously. The basic principle is that the voltage from the bases of Q10 and Q11 to the negative power supply must be equal. Assuming the saturation currents for both of the transistors are equal and neglecting base currents,

\[
R_4 I_{C10} = V_T \ln \left( \frac{I_B}{I_{C10}} \right).
\]

This transcendental equation must be solved iteratively. The answer is

\[
I_{C10} = 18.98 \mu A \approx 19 \mu A.
\]

The current mirror Q12 and Q13 produces two collector currents that are proportional to collector areas. In Q13, the area ratios are such that

\[
I_{C17} = 3I_{C13B} = 0.55 \, \text{mA}
\]

\[
I_{C13A} = \frac{1}{4}I_B = 0.183 \, \text{mA}.
\]

The current mirror Q9 and Q9 produces a current of 19 \( \mu A \) out of the collector of Q8. This current is split evenly between the two halves of Q1,Q2 and Q3,Q4 and Q5,Q6. Thus all these transistors carry \( \frac{1}{2}19 \mu A = 9.5 \mu A \).

The base currents in Q5, Q6, and Q7 are neglected. For Q5,

\[
V_{BE5} = V_T \ln \left( \frac{I_{C10}}{I_S} \right).
\]

If \( I_S = 10^{-14} \, A \) and \( I_{C10} = 9.5 \, \mu A \), then \( V_{BE5} = 537 \, mV \). The voltage across \( R_1 = 1k\Omega \) is 9.5 mV. The voltage across \( R_3 \) is

\[
V_{R3} = V_{BE5} + V_{R1} = 537 + 9.5 = 546.5 \, mV.
\]

Therefore the emitter current of Q7 is

\[
I_{E7} = \frac{546.5 \cdot 10^{-3}}{50 \cdot 10^3} = 10.9 \, \mu A.
\]
Moving on to stage two consisting of Q16 and Q17, the current coming into the collector of Q17 is the already found current \( I_2 = I_{C17} = 550 \mu A \). The voltage at the base of Q17 above the negative power supply is

\[
V_{B17} = I_{C17} R_8 + V_T \ln \left( \frac{I_{C17}}{I_S} \right) = 698 \text{ mV.}
\]

Assuming that npn transistors have \( \beta = 250 \),

\[
I_{B17} = \frac{I_{C17}}{\beta} = \frac{550 \mu A}{250} = 2.2 \mu A.
\]

Then the collector current of Q16 can now be found.

\[
I_{C16} = \frac{V_{B17}}{R_9} + I_{B17} = \frac{698 \cdot 10^{-3}}{50 \cdot 10^3} + 2.2 \cdot 10^{-6}
\]

The analysis of the class B output stage was given previously. In this case Q13A provides bias current of 183\( \mu A \). The output is assumed to be, \( V_{out} = I_{out} = 0 \). With \( I_{C19} = 15.98 \mu A \) and \( I_{C18} = 168 \mu A \) and with the assumption that the areas of the two output transistors Q14 and Q20 are three times larger than the compensation transistors Q18 and Q19, the bias current through the output transistors is

\[
I_{C14} = -I_{C20} = \sqrt{I_{C19} I_{C18}} \sqrt{\frac{I_{S14} I_{S20}}{I_{S18} I_{S19}}} = 155.4 \mu A
\]

Short circuit protection occurs by Q18 and Q21 which are turned on when the current flow through the two small 27\( \Omega \) resistors. These transistors turn on when this voltage drop exceeds about 550 mV (or about 20 mA output current). At this point the base current to the power transistors Q14 or Q20 is shunted to the output.
Below is a summary of the currents.

\[ I_B = 0.73 \text{ mA} \]
\[ I_{C10} = 19 \text{ µA} \]
\[ I_{C13A} = 0.183 \text{ mA} \quad (1/4) \]
\[ I_{C13B} = 0.55 \text{ mA} \quad (3/4) \]
\[ I_C = I_D = 19 \text{ µA} \]
\[ I_{C9} = I_{C8} = 19 \text{ µA} \]
\[ I_{C1} = I_{C2} = I_{C3} = I_{C4} = I_{C5} = I_{C6} = 9.5 \text{ µA} \]
\[ V_{BE5} = 537 \text{ mV} \]
\[ V_{R1} = 9.5 \text{ mV} \]
\[ V_{R3} = 546.5 \text{ mV} \]
\[ I_{E7} = 10.9 \text{ µA} \]
\[ I_{C17} = 0.55 \text{ mA} \]
\[ I_{C16} = 16.2 \text{ µA} \]
\[ I_{C13A} = 0.183 \text{ mA} \]
\[ I_{C19} = 16 \text{ µA} \]
\[ I_{C14} = -I_{C20} = 155.4 \text{ µA} \]

6.4 Small Signal Analysis of the 741 Operational Amplifier

Stage 1

The input stage consists of transistors Q1 . . . Q6. These 6 transistors can be reduced to a model consisting of an input resistance, output resistance and a transconductance. The input is a differential stage and the input resistance can be found from application of Th’evenin’s theorem. The gain is found by methods previously discussed with respect to differential amplifiers. It should be noted that Q1 and Q2 are emitter followers so are characterized as having a high input impedance (as desired). The output resistance as viewed from the collector of Q6 is basically the parallel combination of the output resistances of Q4 and Q6, each with resistors in their emitters. For this circuit,

\[ R_{id} = 2.7 \text{ MΩ} \]
\[ G_{m1} = 0.1838 \text{ mS} \]
\[ 6.79R_{o1} = 6.8 \text{ MΩ} \]

Stage 2

The input resistance, output resistance and gain for the Q16 and Q17 combination is sought. Transistor Q17 is connected as common emitter with emitter degeneration. From the formula sheet,

\[ R_{in17} = r_{\pi17} + R_8(\beta_{17} + 1). \]

The transistor Q16 is an emitter follower with two emitter resistances: the base of Q17 and \( R_9 \). Consequently, the input resistance of the combination is found from the formula sheet.

\[ R_{in16} = r_{\pi16} + (\beta_{16} + 1)(R_{in17}||R_9) \]
This can be evaluated numerically if it is assumed that $\beta_{16} = \beta_{17} = 250$.

$$r_{\pi16} = \frac{\beta_{16}}{I_{C16}} V_T = 406.3 \text{ k}\Omega$$

$$r_{\pi17} = \frac{\beta_{17}}{I_{C17}} V_T = 11.82 \text{ k}\Omega$$

Using these known values,

$$R_{in16} \approx 5.74 \text{ M}\Omega.$$

In calculating the gain, the gain of the emitter follower Q16 is assumed to be 1. The gain of the combination is due to Q17. From the formula sheet, the equivalent transconductance is

$$G_m2 = \frac{g_{m17}}{1 + g_{m17}R_E}.$$ 

Since the value for $g_{m17} = \frac{I_{C17}}{V_T} = 21.15 \text{ mS}$, the transconductance of this stage is

$$G_m2 = 6.79 \text{ mS}.$$ 

The output resistance of this section is the output resistance of Q13B in parallel with that of Q17 and its 100\Omega resistor in its emitter. For the latter, an expression was found from the previous stage. By analogy then,

$$R_{out2} = r_{13B} || \left[ r_{o17} \frac{1 + g_{m17}R_E}{1 + g_{m17}R_E} \right]$$

The Early voltage for Q13A is $V_{AP} = 52$ and for Q17 is $V_{AN} = 130$. Also assuming $\beta_{17} \gg 1$,

$$r_{o13B} = \frac{V_{AP}}{I_{C13B}} = 94.5 \text{ k}\Omega$$

$$r_{o17} = \frac{V_{AN}}{I_{C17}} = 236.4 \text{ k}\Omega$$

$$R_E = 100\Omega$$

$$g_{m17} = 21.15 \text{ mS}$$

$$R_{out2} = 83.75 \text{ k}\Omega$$

**Stage 3**

The input resistance of the third stage does not heavily influence the gain. For calculational purposes, assume a typical load $R_L = 2\text{k}\Omega$. Since Q14 is an emitter follower, its input resistance is

$$R_{in14} = r_{\pi14} + R_L(\beta_{14} + 1)$$

The compensation transistors Q18 and Q19 can be adequately modeled simply as two series diodes D18 and D19 for the purpose of finding the AC equivalent circuit. From the
emitter of Q23, there are three resistances in series which can be named for the moment as $R_b$.

$$R_b = r_{d18} + r_{d19} + (r_{o13A} || R_{in14})$$

The input resistance then looking into the emitter follower of Q23 is the input resistance of this third section.

$$R_{in3} = r_{\pi23} + R_b(\beta_{23} + 1)$$

Evaluation of this gives $R_{in3} = 9.297 \, M\Omega$. As desired, $R_{in3} >> R_{out2}$ so the second stage (and hence the gain) is not significantly affected by the loading of the output stage.

The output resistance, $R_{out3}$ is found by looking into the emitter of Q14. The resistance seen by the base of Q14 looking back toward the input is $R_c$.

$$R_c = r_{o13A} || (r_{d18} + r_{d19} + R_{o23})$$

$R_{o23} = \frac{R_{out2} + r_{\pi23}}{\beta_{23} + 1}$ so that

$$R_{out3} = \frac{R_c + r_{\pi14}}{\beta_{14} + 1} = 21.12 \, \Omega$$

To this add the current limiting transistor of 27Ω and the result is

$$R_{out} = 48 \, \Omega$$

The final stage is modeled then with an input resistance $R_{in3} = 9.29 M\Omega$, a voltage controlled voltage source with gain of 1 and a series output resistance of 48Ω.

**The full Amplifier Gain**

The voltage gain of the total amplifier is the cascaded combination of the three stages. The gain of the last stage, being an emitter follower is 1.

$$A_v = [G_{m1} (R_{out1} || R_{in2})] [(G_{m2} (R_{out2} || R_{in3}))]$$

$$A_v = [576.45][563.6] = 324,880$$

$$R_{in} = R_{id} = 2.7 \, M\Omega$$

$$R_{out} = 48 \, \Omega$$

This was a first order approximation. The bias currents are typically 10% to 30% higher in actual operational amplifiers. In this analysis several assumptions were made, among them high values for $\beta$ and $r_o$ at certain places. Actual $\beta$s are lower than those used here in some places because of the small bias currents.
The $\mu$A741 operational amplifier has been a standard operational amplifier for many decades. However, it typically runs with two power supplies at $\pm 15$ volts. Today’s applications often require a single power supply with lower voltages (s to 5 volts). The NE 5234 operational amplifier is capable of fulfilling these twin goals. However, the common mode input voltage becomes a critical factor especially when operating near 0 volts.

The input stage for the NE5234 is a folded cascode circuit. A generic form for this circuit is shown below. This is the same as Fig. 6.33 except the transistor names are changed to have the same form of the more complete model in Fig. 6.36. Transistors $Q6$, and the rest of them must be biased to ensure they remain in their active mode.

Transistor $Q6$ is biased by adding $Q7$, $Q8$, and $Q12$ to provide stable operation of the $n\!p\!n$ input pair.
In these circuits, the resistor values are chosen to provide approximately 200 mV voltage drop. The resistor values are $R_6 = 10 \, \text{k\Omega}$, $R_7 = 10 \, \text{k\Omega}$, $R_8 = 33 \, \text{k\Omega}$, $R_9 = 22 \, \text{k\Omega}$, $R_{10} = 22 \, \text{k\Omega}$, $R_{11} = 33 \, \text{k\Omega}$, $R_{12} = 66 \, \text{k\Omega}$, $R_{13} = 33 \, \text{k\Omega}$, and $R_{14} = 33 \, \text{k\Omega}$,