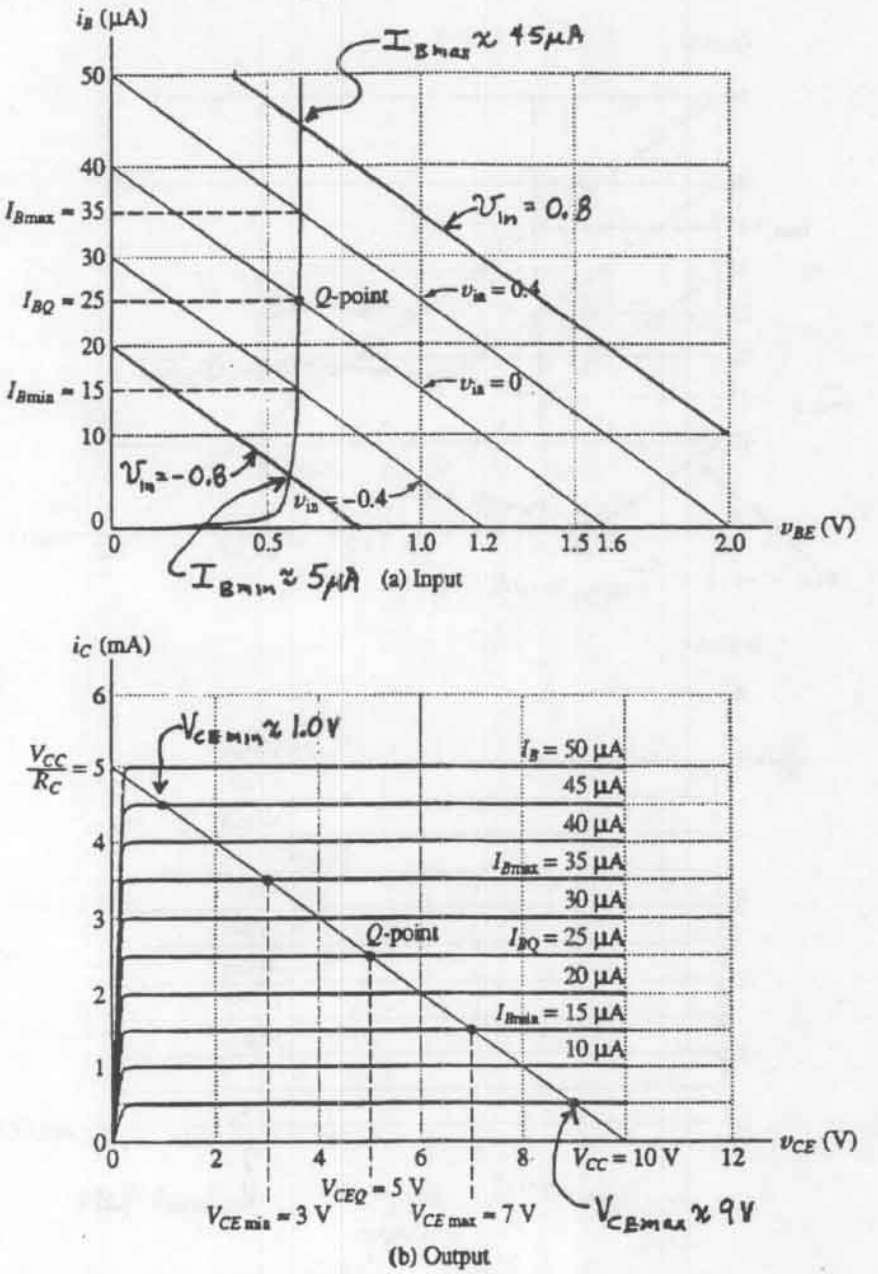
Exercise 4.5

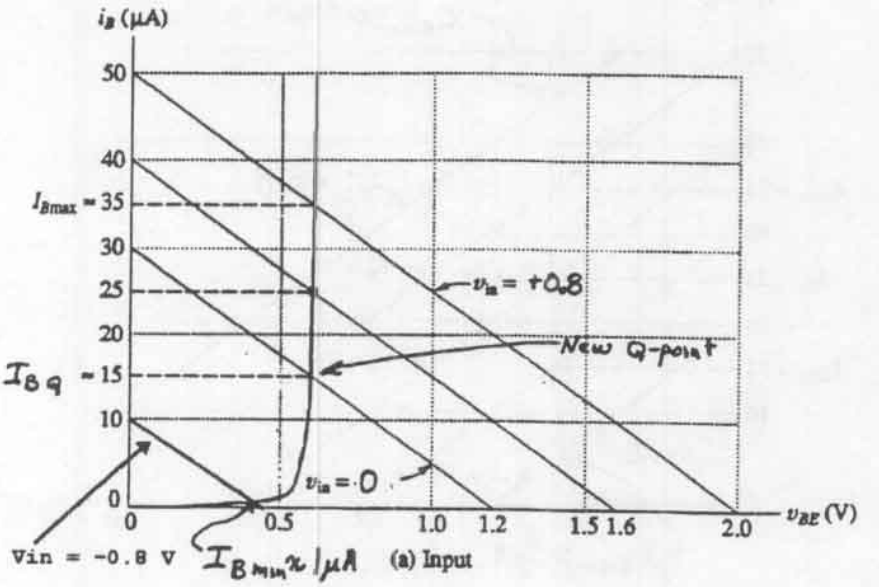
The load lines for v_{in} = -0.8 V and 0.8 V are shown below.

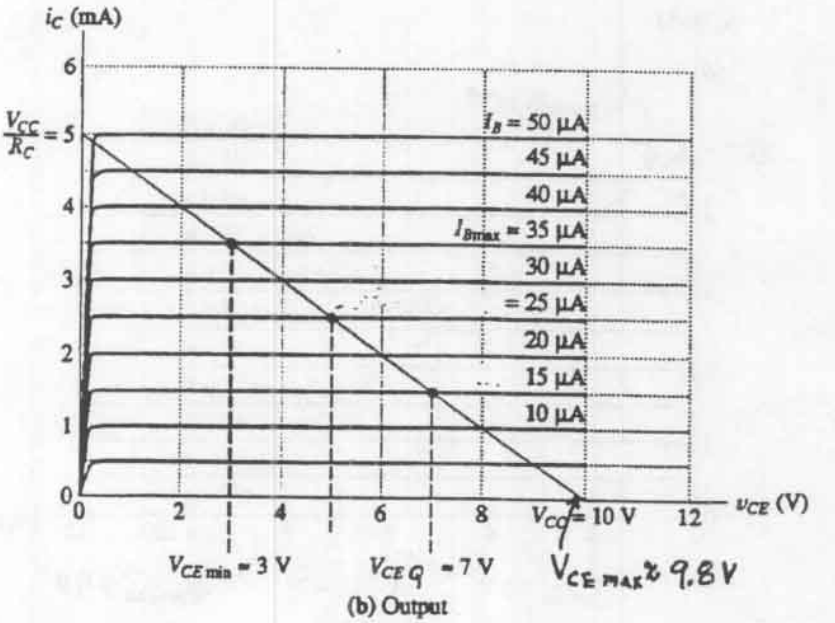


The results are $V_{CEmax} \cong 9.0$ V, $V_{CEQ} \cong 5.0$ V, $V_{CEmin} \cong 1.0$ V.

Exercise 4.6

The load lines are shown below.





From the load lines we find $V_{CEmax} \cong 9.8$ V, $V_{CEQ} \cong 7.0$ V, and $V_{CEmin} \cong 3.0$ V.

Exercise 4.9

(a) $V_{BE} = -0.2$ V and $V_{CE} = 5$ V, because we have $v_{BE} < 0.5$, the transistor is in cutoff.

(b) $I_B = 50\ \mu A$ and $I_C = 2$ mA, because we have $I_C < \beta I_B$ the transistor is in saturation.

(c) $V_{CE} = 5$ V and $I_B = 50\ \mu A$, because we have $V_{CE} > 0.2$ and $I_B > 0$, the transistor is in the active region.

Exercise 4.13

$$R_1 = 100\ k\Omega \qquad R_2 = 50\ k\Omega$$

$$R_B = \frac{1}{1/R_1 + 1/R_2} = 33.3\ k\Omega$$

$$V_B = V_{CC}\frac{R_2}{R_1 + R_2} = 5\ V$$

$$I_B = \frac{V_B - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{5 - 0.7}{33.3k + (\beta+1)1k}$$

$$I_C = \beta I_B$$

$$I_E = I_C + I_B$$

$$V_{CE} = V_{CC} - R_C I_C - R_E I_E$$

β	I_B (μA)	I_C (mA)	I_E (mA)	V_{CE} (V)
100	32.0	3.20	3.23	8.57
300	12.9	3.86	3.87	7.27

In Example 4.7 the ratio of the collector currents is 4.24/4.12 = 1.029. For the higher resistor values in this exercise the ratio is 3.86/3.20 = 1.21. In general higher resistance values in the four-resistor bias circuit lead to

greater changes in the bias point with changes in β. The SPICE simulation is stored in the file named Exer4_13.