EE 5305
Problem Set #2
Due Wednesday September 15, 2010

Problems from Chapter 1 in Gray, Hurst, Lewis & Meyer
Read sections 1.1, 1.2.x, 1.3.x, 1.4.x, 1.5, 1.5.1, 1.5.2, 1.5.3, 1.6, 1.6.1, 1.6.2, 1.6.3, 1.6.4,
1.6.5, 1.6.6, 1.6.8, Appendix A.1.1, Appendix A.2.1 (p. 163 in chapter 2)

1. Problem 1.5. Note: for Si $\epsilon_r = 11.7$.

2. Problem 1.8. In addition, calculate the maximum low frequency gain and the maximum
frequency where oscillation could occur.

3. Problem 1.9. This is a repeat of 1.8 only with higher collector current. Again find the
gain and maximum frequency of oscillation.

4. Problem 1.10 The best way of sketching the results is to create a small signal model in
PSPICE using the parameters from 1.8 and 1.9 above. Determination where the current
gain goes to 0 dB determines $f_t$. Which device would you expect to have the highest $f_t$?
The problem statement says to “sketch.” This should be replaced by the word “plot” where
you calculate numbers and make a graph.

5. What change in $V_{BE}$ in a bipolar transistor will cause a ten fold increase in the collector
current. Assume the ideality factor is 1.